IN THE CLAIMS:

Please amend claims 1 through 19 as follows:

1. (Amended) A semiconductor testing apparatus for testing semiconductor devices comprising:

a read circuit configured to read measurement data including a test vector data and data of good samples and data of faulty samples returned to a manufacturer;

a determination circuit configured to supply the test vector data to the good samples and the faulty samples, and to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and

an IDDQ measuring circuit configured to test semiconductor devices by applying the effective test vector.

2. (Amended) The apparatus of claim 1 wherein the determination circuit comprises:

a changing rate calculation circuit configured to select address pairs from the test vector data, to supply the address pairs to the good samples and the faulty samples, to measure current-values of the good samples and faulty samples, and to calculate changing rates of each of the good samples and faulty samples;

a range criteria determination circuit configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

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a comparing circuit configured to compare the changing rates of each of the faulty samples to the range of pass/fail decision criteria, and to determine whether the changing rates of each of the faulty samples fall outside of the range of the pass/fail decision criteria; and

an effective address pair determination circuit configured to determine the changing rate falling outside of the range of pass/fail decision criteria, and to select an address pair which makes the faulty samples provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

3. (Amended) The apparatus of claim 1, wherein the IDDQ measuring circuit comprises:

a tester configured to: acquire the effective address pair, supply test vectors corresponding to the effective address pair to the semiconductor device, measure current-value output of the semiconductor device, and calculate changing rates of the semiconductor device; and

a decision circuit configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

4. (Amended) The apparatus of claim 1 further comprising a display configured to display the changing rate falling outside of the range of pass/fail decision criteria.

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5. (Amended) A semiconductor testing method for testing semiconductor devices, comprising:

reading measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer;

supplying the test vectors to the good samples and the faulty samples;

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and

applying test vectors of the effective address pairs to the semiconductor devices for testing.

6. (Amended) The method of claim 5, further comprising:

selecting address pairs from the test vector data;

supplying the address pairs to the good samples and the faulty samples;

measuring current-values of the good samples and the faulty samples;

calculating changing rates of each of the good samples and the faulty samples;

determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

comparing the changing rates of each of the faulty samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the faulty samples fall outside of the range of pass/fail decision criteria;

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determining the changing rate falling outside of the range of pass/fail decision criteria; and

selecting an address pair which makes the faulty samples provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

7. (Amended) The method of claim 5, further comprising:

acquiring the effective address pair;

supplying test vectors corresponding to the effective address pair to the semiconductor devices;

measuring current-value output of the semiconductor devices;

calculating change rates of the semiconductor devices; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

8. (Amended) The method of claim 7, further comprising displaying the changing rate falling outside of the range of pass/fail decision criteria on a display.

9. (Amended) A program with which a semiconductor testing method for testing semiconductor devices is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, an IDDQ measuring circuit, the program comprising:

instructions configured to read measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer;

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instructions configured to supply the test vector data to good samples and faulty samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and

instructions configured to apply test vectors of the effective address pairs for testing.

10. (Amended) The program of claim 9, further comprising:

instructions configured to select address pairs from the test vector data;

instructions configured to supply the address pairs to the good samples and the faulty samples

instructions configured to measure current-values of the good samples and the faulty samples;

instructions configured to calculate changing rates of each of the good samples and the faulty samples;

instructions configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

instructions configured to compare the changing rates of each of the faulty samples to the range of pass/fail decision criteria;

instructions configured to determine whether the changing rates of each samples fall outside of the range of pass/fail decision criteria;

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instructions configured to determine the changing rate falling outside of the range of pass/fail decision criteria; and

instructions configured to select an address pair that makes the faulty samples to provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

11. (Amended) The program of claim 9, further comprising:

instructions configured to acquire the effective address pair;

instructions configured to supply test vectors corresponding to the effective address pair to the semiconductor devices;

instructions configured to measure current-value output of the semiconductor devices;

instructions configured to calculate changing rates of the semiconductor devices; and

instructions configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

12. (Amended) The program of claim 11, further comprising instructions configured to display the changing rate falling outside of the range of pass/fail decision criteria on a display.

13. (Amended) A semiconductor testing method of specifying a faulty part in a semiconductor device, comprising:

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reading measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

supplying test vector data to good and faulty samples;

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

applying test vectors of the effective address pairs to a semiconductor device; and

specifying a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

14. (Amended) The method of claim 13, further comprising:

selecting address pairs from the test vector data;

supplying the address pairs to the good samples and the faulty samples;

measuring current-values of the good samples and faulty samples;

calculating changing rates of each of the good samples and faulty samples;

determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

comparing the changing rates of each of the faulty samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the faulty samples fall outside of the range of pass/fail decision criteria;

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determining the changing rate falling outside of the range of pass/fail decision criteria; and

selecting an address pair which makes the faulty samples provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

15. (Amended) The method of claim 14, wherein the faulty part specifying step further comprises:

acquiring the effective address pair;

supplying test vectors corresponding to the effective address pair to the semiconductor device;

measuring current-value output of the semiconductor device;

calculating changing rates of the semiconductor device;

measuring an emission from the semiconductor device; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

16. (Amended) A semiconductor testing apparatus for specifying a faulty part in a semiconductor device, comprising:

a read circuit configured to read measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

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a determination circuit configured to supply the test vector data to the good samples and faulty samples, and to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process; and

a faulty part specifying circuit configured to apply test vectors of the effective address pairs to a semiconductor device and to specify a faulty part by measuring an emission from the semiconductor device.

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17. (Amended) The method of claim 13, wherein determining a range of pass/fail decision criteria is achieved by:

a changing rate calculation circuit configured to select address pairs from the test vector data, to supply the address pairs to the good samples and the faulty samples, to measure current-values of the good samples and faulty samples, and to calculate changing rates of each of the good samples and faulty samples;

a range criteria determination circuit configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

a comparing circuit configured to compare the changing rates of each of the faulty samples to the range of pass/fail decision criteria, and to determine whether the changing rates of each of the faulty samples fall outside of the range of pass/fail decision criteria; and

an effective address pair determination circuit configured to determine the changing rate falling outside of the range of pass/fail decision criteria, and to select an

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address pair that makes the faulty samples to provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

18. (Amended) The method of claim 17, wherein the faulty part specifying circuit further comprises:

a tester configured to acquire the effective address pair, to supply test vectors corresponding to the effective address pair to the semiconductor device, to measure current-value output of the semiconductor device, and to calculate changing rates of the semiconductor device;

an emission measuring circuit configured to measure an emission from the semiconductor device; and

a decision circuit configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

19. (Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, the program comprising:

instructions configured to read measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

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